

REMARKS

This amendment is filed in response to the Office Action filed on Oct. 24, 2001.
All objections and rejections are respectfully traversed.

Claims 1-34 are in the case.

Claims 21-34 were added to better claim the invention.

Claim Rejections – 35 U.S.C. §102

At paragraph 2 of the Office Action claims 1-6, 10-12, and 15 were rejected under 35 U.S.C. §102 as being unpatentable in view of Narad et al., US patent No. 6,157,955 issued on Dec 5, 2000, hereinafter Narad.

The present invention as set forth in representative claim 1 comprises in part:

1. Apparatus for tightly-coupling hardware data encryption functions with software-based protocol decode processing within a pipelined processor of a programmable processing engine in a network switch, the apparatus comprising:

an *encryption execution unit contained within the pipelined processor*; and

a software and hardware interface that enables the encryption execution unit to efficiently cooperate with resources of the pipelined processor.

The Narad patent describes a packet-processing system that accelerates network infrastructure applications by employing a three-tier approach to filtering packets (col 7, lines 7-10). Packets are first run through a classification engine that executes hardware assist operations such as chained field comparisons (col 6, lines 62-66). Packets are then handed to a policy processor, a microprocessor that executes policy decisions such as to pass, drop, enqueue, etc... (col. 6 line 66 to col 7, line 2). Packets that require additional processing are sent to an application processor, a general purpose microprocessor (col 7,

lines 2-4 and col 3, lines 66-67) and/or **an external cryptography (“Crypto”) co-processor** (col 8, lines 1-2 and col 26 lines 65-67 and Fig. 3, item 246). The Crypto co-processor obtains packets from a buffer, performs its operation, and then writes the result to back to a memory address (col 27, lines 10-29).

Applicant respectfully urges that Narad does not show Applicant’s claimed novel ***“encryption execution unit contained within the pipelined processor.”***

The Narad patent describes the Crypto co-processor as an external and separate processor. There is absolutely no disclosure of including the Crypto unit within another processor that performs protocol decode functions. Further, because the Crypto unit is located externally and reads and writes from internal buffers and memory, substantial data movement must occur over system buses. This particular limitation is novelly overcome by the Applicant’s design.

Applicant respectfully urges that the Narad patent is legally precluded from anticipating the claimed invention under 35 U.S.C. §102 because of the absence from the Narad patent of Applicant’s ***“encryption execution unit contained within the pipelined processor.”***

Claim Rejections – 35 U.S.C. §103

At paragraph 5 of the Office Action claim 20 was rejected under 35 U.S.C. 103(a) as being unpatentable over Narad in view of Key et al., US patent No. 6,173,386 issued on Jan 9, 2001, hereinafter Key.

Key describes a parallel processor with a plurality of processors, each of which having integrated debug capabilities. The processors are arranged in an array of rows and columns, and connected to input and output head buffers. When entered into a special debug mode, the internal states of processors can be examined for debugging purposes (col 5, lines 39-43).

Applicant respectfully urges that neither Narad nor Key show Applicant's claimed novel "*encryption execution unit contained within the pipelined processor.*"

There is absolutely no disclosure in Key relating to locating an encryption execution unit internal to a processor, nor even reference to encryption in general.

Applicant respectfully urges that the Narad patent and the Key patent, either taken singly or taken in any combination, are legally insufficient to render the presently claimed invention obvious under 35 U.S.C. §103 because of the absence in each of the cited patents of Applicant's claimed novel "*encryption execution unit contained within the pipelined processor.*"

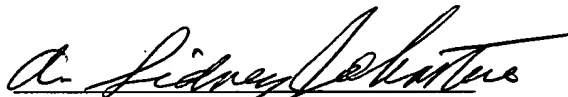
All independent claims are believed to be in condition for allowance.

All dependant claims are believed to be dependent from allowable independent claims.

Favorable action is respectfully solicited.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,



A. Sidney Johnston
Reg. No. 29,548
CESARI AND MCKENNA, LLP
88 Black Falcon Avenue
Boston, MA 02210-2414
(617) 951-2500

**MARK-UP PAGES FOR THE JANUARY 18,
2002, AMENDMENT TO U.S. PATENT AP-
PLICATION SER. NO. 09/216,519**

The replacement for the FIRST full paragraph of page PAGE resulted from the following changes:

COPY PARAGRAPH TO BE AMENDED HERE.

The replacement for claim CLAIM resulted from the following changes:

COPY CLAIM TO BE AMENDED HERE.